

Attorney Docket No. 5649-1114

TT21
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APR 29 2005

In re: Hideki
Application Serial No.: 10/617,958
Filed: July 11, 2003
For: *Phase Changeable Memory Devices Having Reduced Cell Areas*

U.S. Patent No.: 6,849,892
Issued: February 1, 2005

Date: April 27, 2005

Commissioner for Patents
Attn: Certificate of Correction Branch
P.O. Box 1450
Alexandria, VA 22313-1450

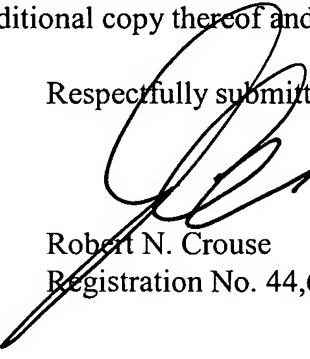
**REQUEST FOR ENTRY OF CERTIFICATE OF CORRECTION UNDER
35 U.S.C §254 AND 37 C.F.R. §1.322**

Sir:

The Assignee of record for the above-referenced patent hereby requests, pursuant to 35 U.S.C §254 and 37 C.F.R. §1.322, that a Certificate of Correction be issued. This request is made in order to correct the mistakes incurred through the fault of the U.S. Patent and Trademark Office. No fee is believed due. However, the Commissioner is authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-0220.

The mistakes appearing in the patent are set forth with corrections on the Certificate of Correction enclosed herewith, with an additional copy thereof and a return post card.

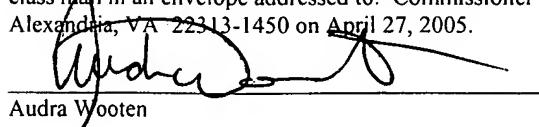
Respectfully submitted,


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Certificate of Mailing under 37 CFR 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Attn: Certificate of Correction Branch, P.O. Box 1450, Alexandria, VA 22313-1450 on April 27, 2005.


Audra Wooten

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO. : 6,849,892

DATED : February 1, 2005

INVENTOR(S) : Hideki

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims:

Column 16, line 16 should read -- are about half of the width of the transistor active region. --

Column 16, line 33 should read -- region and wherein the second storage region protrudes from --

Column 16, line 36 should read -- 5. A device according to claim 1 wherein the transistor --

MAILING ADDRESS OF SENDER:

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PATENT NO. 6,849,892

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This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you are required to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.